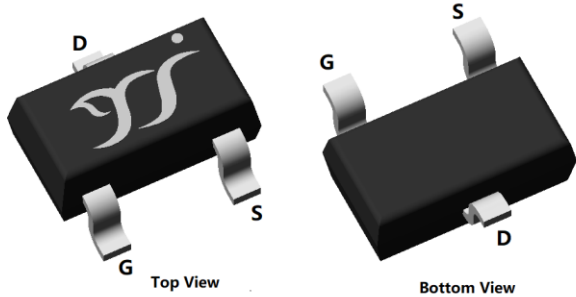
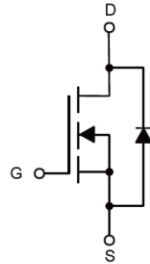


## N-Channel Enhancement Mode Field Effect Transistor



**SOT-23-3L**



### Product Summary

- $V_{DS}$  60V
- $I_D$  3A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $< 85m\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ )  $< 95m\Omega$

### General Description

- Trench Power LV MOSFET technology
- High Speed switching
- Halogen Free
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Power switching application
- PWM application

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_A=25^\circ C$	3
		$T_A=100^\circ C$	1.9
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	18	A
Total Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ C$	1.2
		$T_A=100^\circ C$	0.45
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>C</sup>	$R_{\theta JA}$	85	105	$^\circ C/W$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL03N06AL	F2	S10.	3000	30000	120000	7" reel



# YJL03N06AL

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =60V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.9	1.35	2	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3A	-	62	85	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A	-	70	95	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =0V	-	0.85	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz, Open drain	-	2	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	3	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz	-	500	-	pF
Output Capacitance	C <sub>oss</sub>		-	28	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	22	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =3A	-	10	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.7	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	2.1	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =3A, di/dt=100A/us	-	7	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	33	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, R <sub>L</sub> =20Ω R <sub>GEN</sub> =3Ω	-	3.6	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	17.6	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	13	-	
Turn-off fall Time	t <sub>f</sub>		-	23	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R<sub>θJA</sub> is measured with the device mounted on the minimum recommend pad size, in the still air environment with T<sub>A</sub>=25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



Typical Electrical and Thermal Characteristics Diagrams

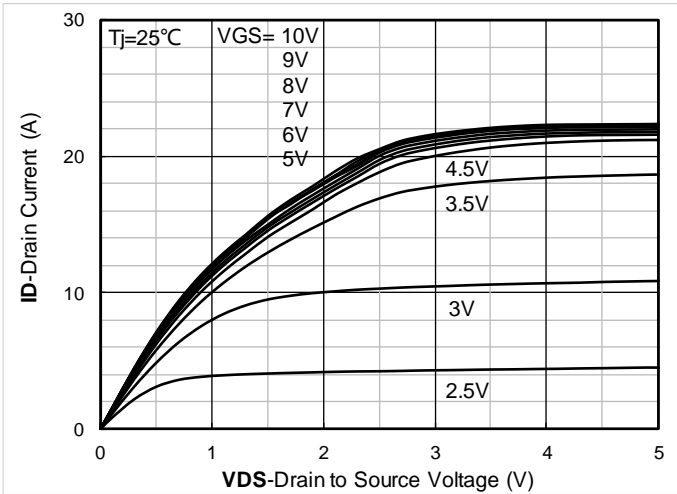


Figure 1. Output Characteristics

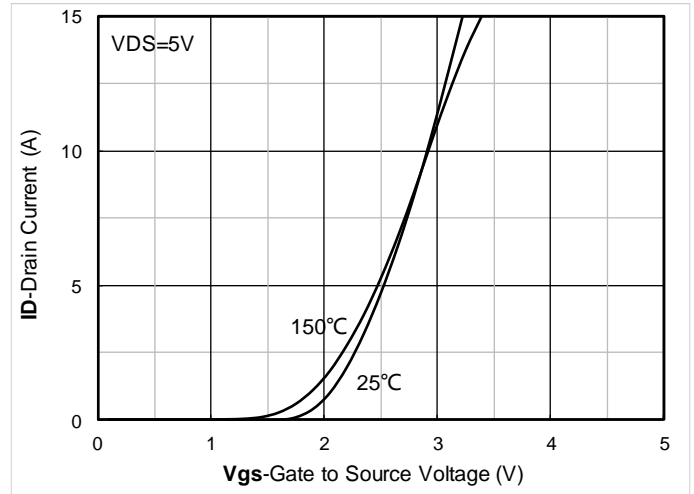


Figure 2. Transfer Characteristics

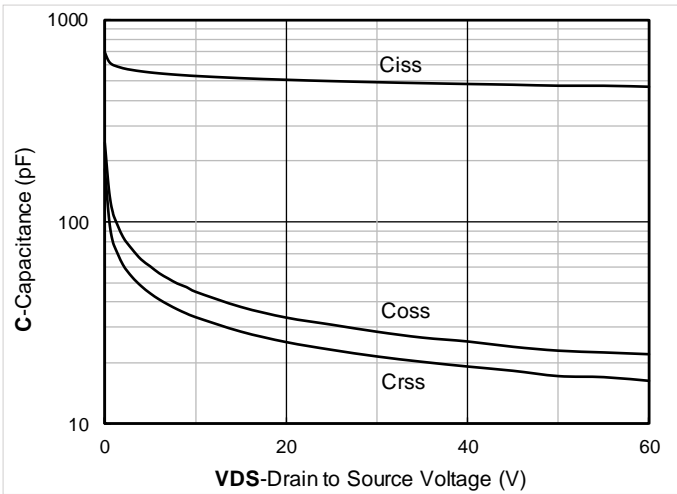


Figure 3. Capacitance Characteristics

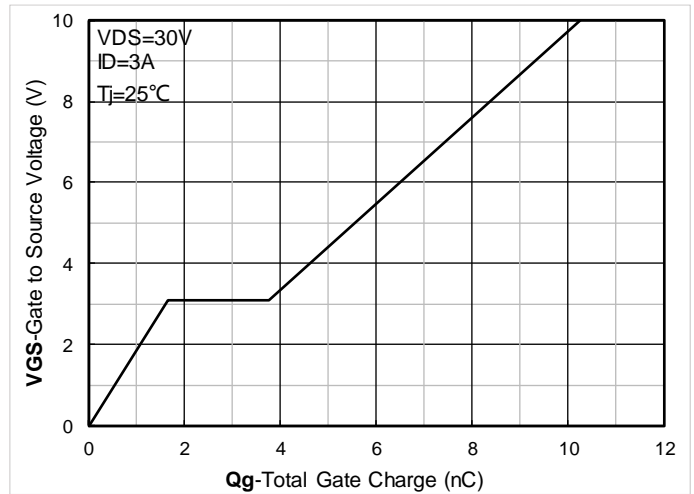


Figure 4. Gate Charge

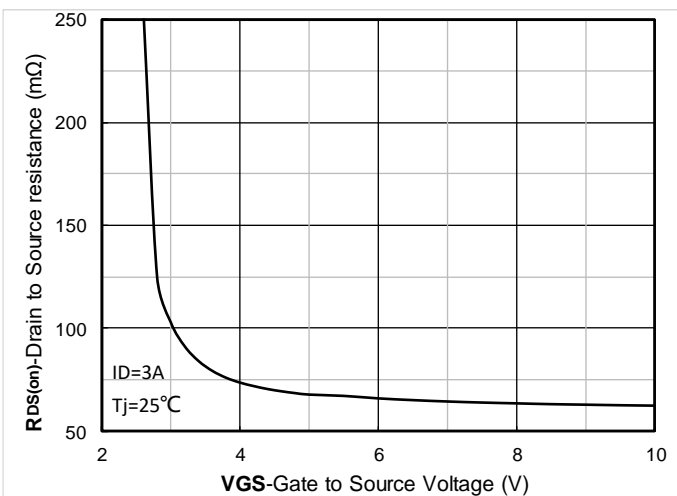


Figure 5. On-Resistance vs Gate to Source Voltage

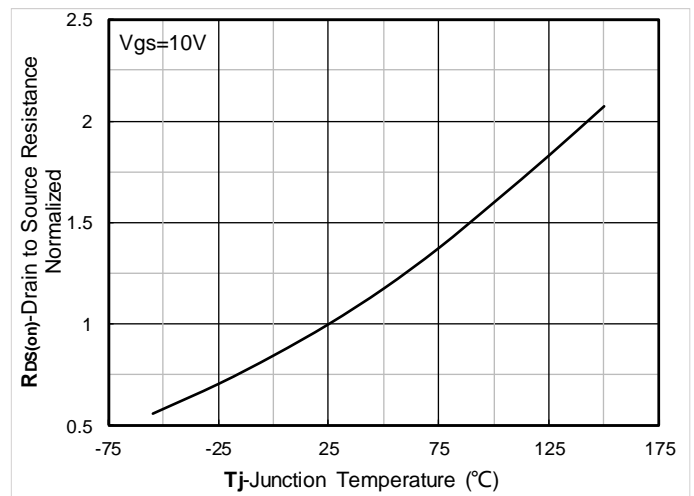


Figure 6. Normalized On-Resistance



# YJL03N06AL

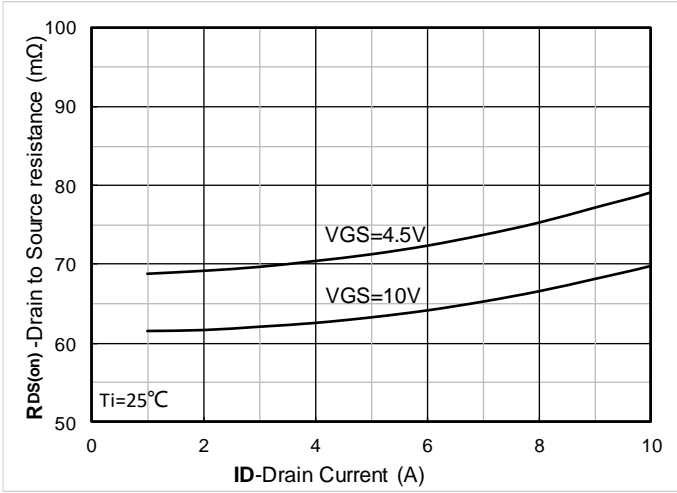


Figure 7.  $R_{DS(on)}$  VS Drain Current

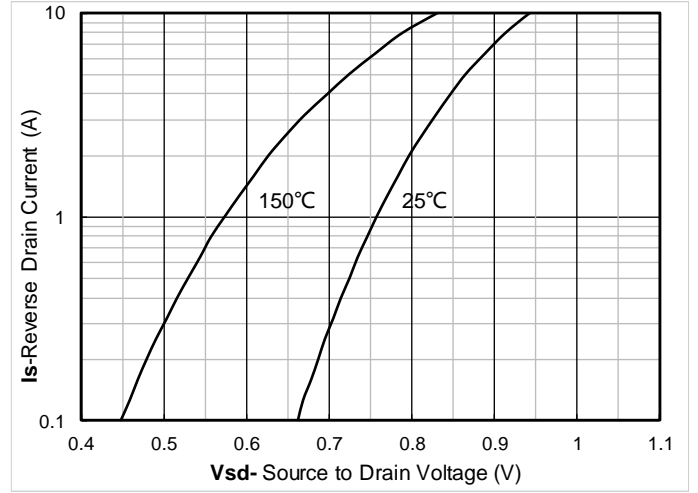


Figure 8. Forward characteristics of reverse diode

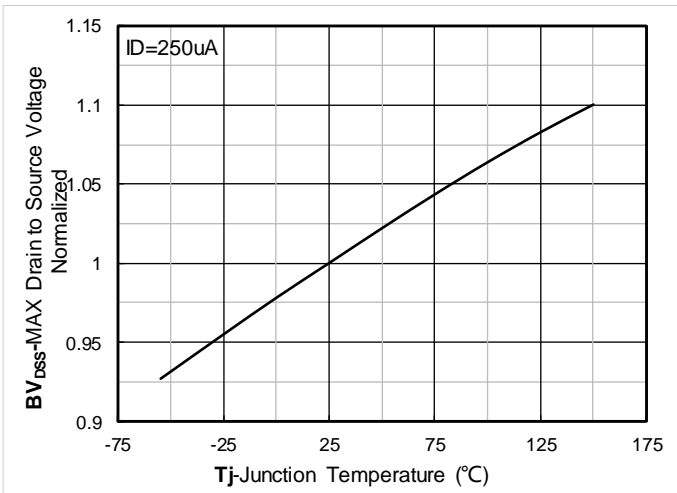


Figure 9. Normalized breakdown voltage

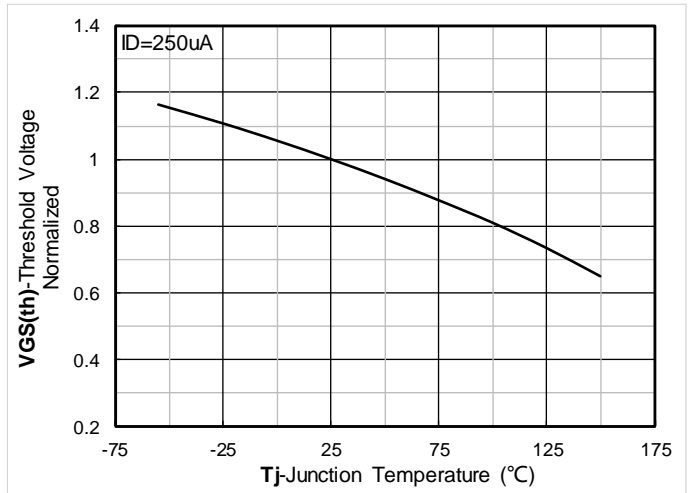


Figure 10. Normalized Threshold voltage

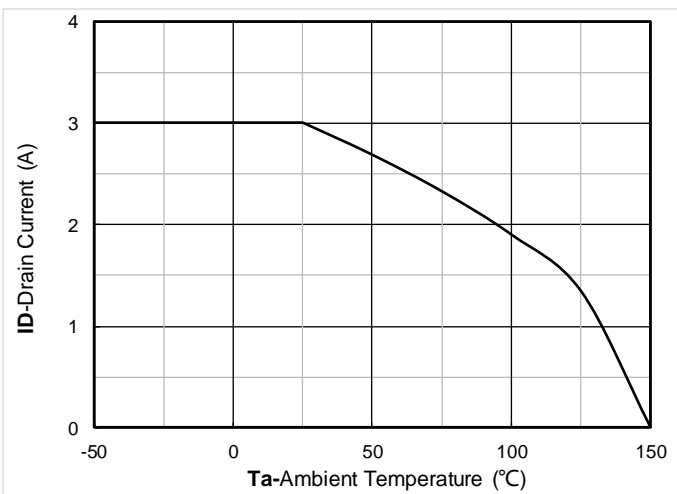


Figure 11. Current dissipation

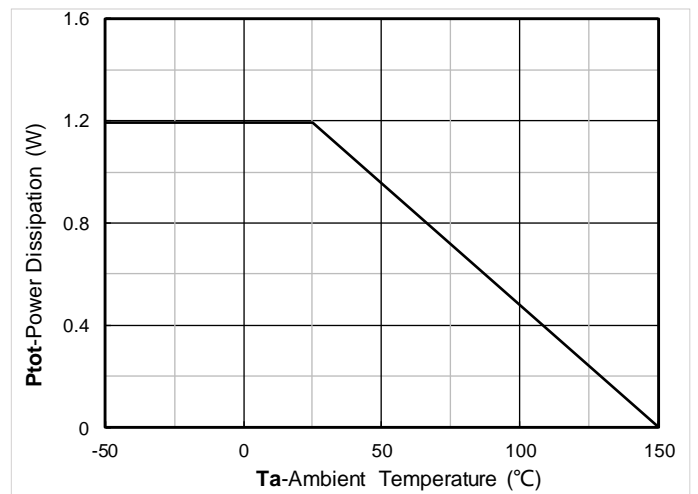


Figure 12. Power dissipation

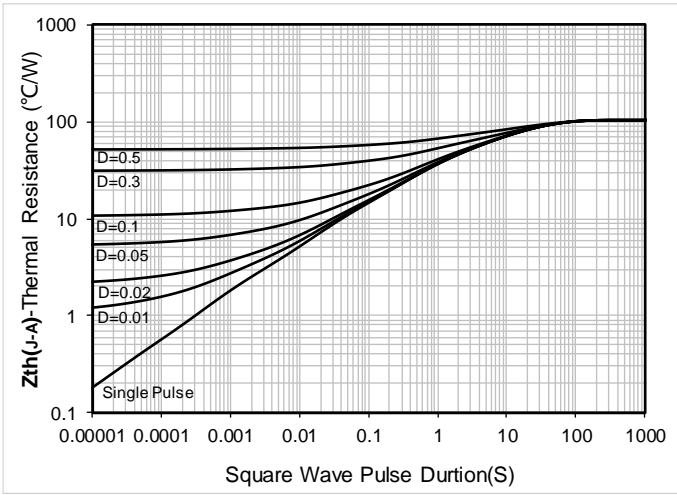


Figure 13. Maximum Transient Thermal Impedance

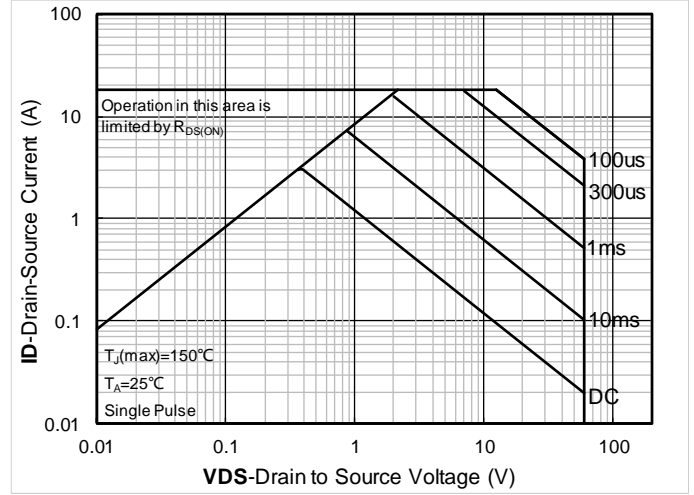


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

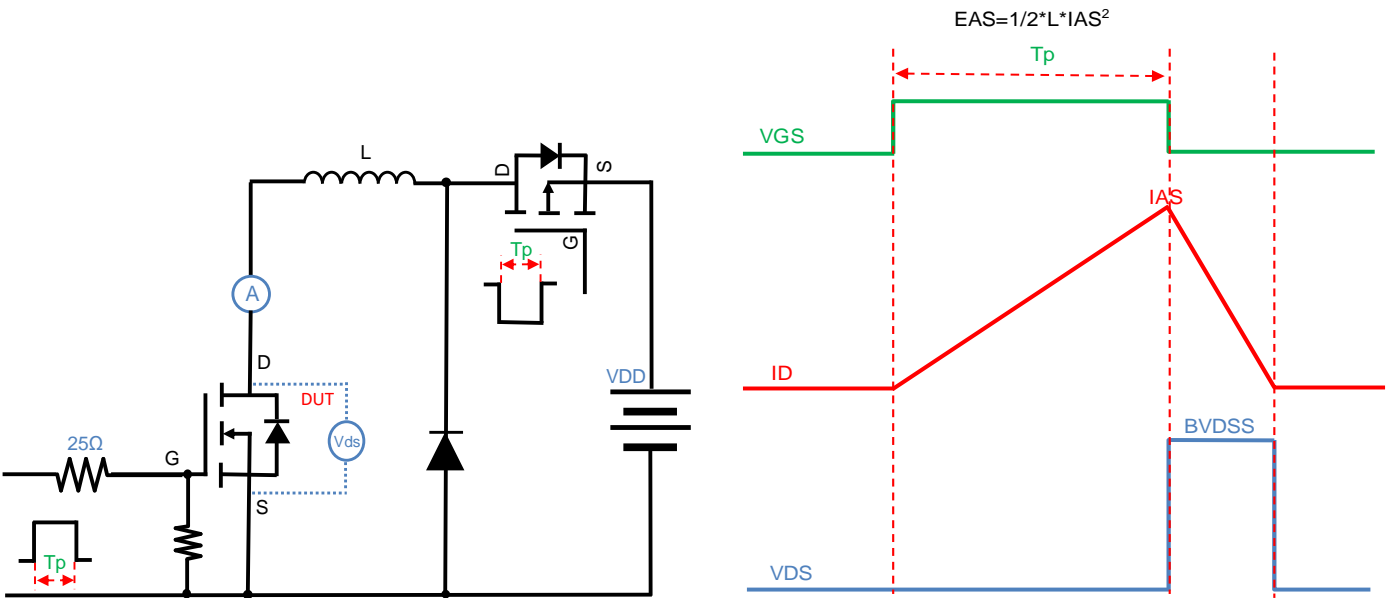


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Figure B. Gate Charge Test Circuit & Waveform

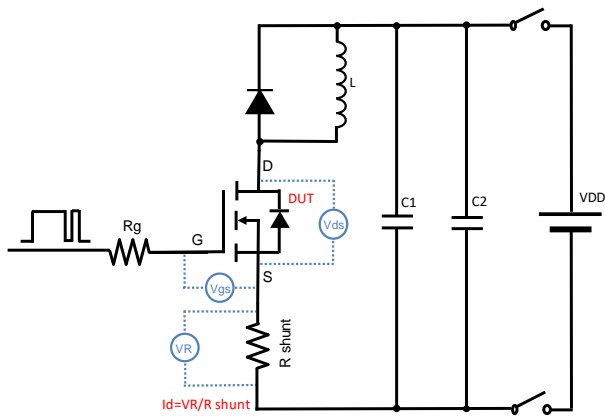
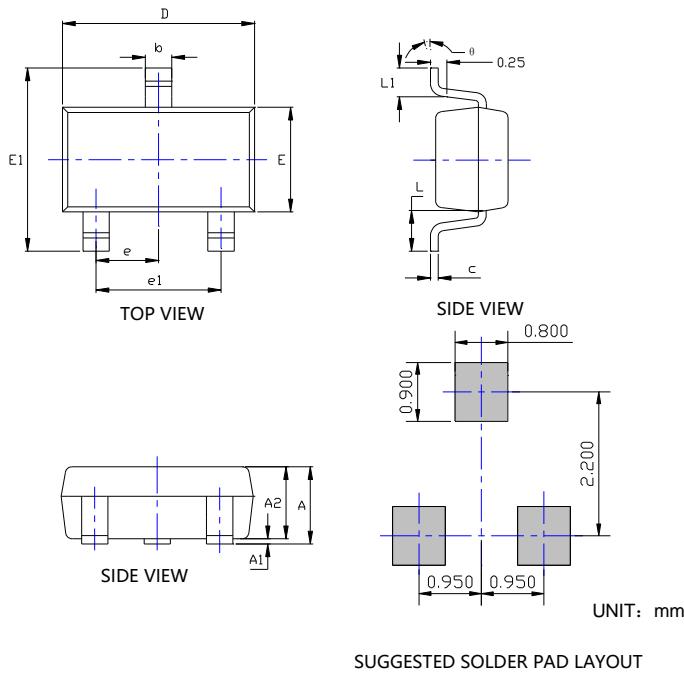


Figure C. Resistive Switching Test Circuit & Waveform



Figure D. Diode Recovery Test Circuit & Waveform

## ■ SOT-23-3L Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.041	---	0.049	1.050	---	1.250
A1	0.000	---	0.008	0.000	---	0.200
A2	0.041	0.043	0.045	1.050	1.100	1.150
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.111	0.115	0.119	2.820	2.920	3.020
E	0.059	0.063	0.067	1.500	1.600	1.700
E1	0.104	0.110	0.116	2.650	2.800	2.950
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.024REF			0.600REF		
L1	0.012	0.018	0.024	0.300	0.450	0.600
θ	0°	---	8°	0°	---	8°

**NOTE:**

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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